09/159,748.

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PTO/SB/21 (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	Patent#: 7,149,663
Filing Date	Issued: December 12, 2006
First Named Inventor	Geoff Barrett
Art Unit	2123
Examiner Name	W. D. Thomson
Total Number of Pages in This Submission	
Attorney Docket Number	S1022.80126US00

ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [x] Request for Certificate of Correction
- [x] Certificate of Correction
- [x] Copy of Column 8 of U.S. Patent No. 7,149,663
- [x] Copy of Page 5 of Amendment Filed November 9, 2005
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
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- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature			
Printed name	James H. Morris		
Date	December 21, 2006	Reg. No.	34,681

Certificate of Mailing Under 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: December 21, 2006

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Signature			
Printed name	James H. Morris		
Date	December 21, 2006	Reg. No.	34,681

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Dated: December 21, 2006

Signature: _____ (Eileen M. MacKenzie)

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Docket No.: S1022.80126US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Geoff Barrett		
Serial No.:	09/159,748	Patent No.:	7,149,663
Filed:	September 23, 1998	Issued	December 12, 2006
For:	METHOD AND APPARATUS FOR RESTRUCTURING A BINARY DECISION DIAGRAM		
Examiner:	W. D. Thomson		
Art Unit:	2123	Confirmation No.	5513

Certificate of Mailing Under 37 CFR 1.8(a)
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Dated: December 21, 2006

Eileen M. MacKenzie

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted a typographical error which should be corrected.

In the Claims:

In Claim 8, found in column 8, line 13, the word "in" has been omitted between "of the binary decision diagram" and "a representation of a".

The error, omission of the word "in", was not in the application as filed by Patentee. Further, the word "in" was not deleted by any amendment by either the Patentee or Examiner.

In support of the above request, Patentee submits a highlighted copy of page 5 of the amendment filed on November 9, 2005, showing claim 8 as pending, and column 8 of U.S. Patent No. 7,149,663, showing the omission.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: December 21, 2006

Respectfully submitted,

By: _____

James H. Morris
Registration No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
(617) 646-8000

6. An apparatus for restructuring a binary decision diagram representative of a hardware system, comprising:

storage circuitry for storing bits representative of a set of functions as a binary decision diagram corresponding to the hardware system, the binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes; and

a processor adapted to detect a number of nodes of the binary decision diagram, and in response to the detection,

arranging the variables of the binary decision diagram in a representation of a graph having a top, nodes and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes,

traversing the representation of the graph from the top down, to produce a list of the labels in a selected order, and

sifting the variables of the binary decision diagram based on the selected order, wherein the sifted variables are written by the processors to the storage circuitry.

7. A method for proving the properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine variables of the internal signals, the method comprising acts of:

representing the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

substituting the functions which determine the variables of the internal signals;

arranging the variables of the binary decision diagram in a representation of a graph having a top, nodes and leaves, the nodes being labeled with the variables of the system and the leaves being labeled with a set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes;

traversing the representation of the graph from the top down to produce a list of the labels in a selected order; and

sifting the variables of the binary decision diagram based on the selected order.

8. An apparatus for proving properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine values of the internal signals, the apparatus comprising:

first storage circuitry for storing bits representative of a set of functions which represent the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

a processor that substitutes the functions which determine the values of the internal signals into the set of functions representing the system and detects an increase in a number of the nodes of the binary decision diagram, and in response to the detection, arranges the variables of the binary decision diagram in a representation of a graph having a top, nodes and leaves, the nodes being labeled with the set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes, traverses the labels in a selected order and sifts the variables of the binary decision diagram based on the selected order; and

second storage circuitry, wherein the sifted variables of the binary decision diagram are written by the processor to the second storage circuitry.

9. The apparatus of claim 8, wherein the number is a threshold derived from an original number of nodes.

10. Apparatus as claimed in claim 8, wherein the number is a number of nodes which branch on a predetermined variable.

11. The apparatus of claim 8, wherein the number is an absolute number.

12. The method of claim 1, wherein one or more of the acts of arranging, traversing and using are implemented using a computer.

13. The method of claim 12, wherein the acts of arranging, traversing and using are implemented using a computer.

14. The method of claim 3, wherein one or more of the acts of arranging, traversing, sifting and restructuring are implemented using a computer.

15. The method of claim 14, wherein the acts of arranging, traversing, sifting and restructuring are implemented using a computer.

16. The method of claim 7, wherein one or more of the acts of arranging, traversing and sifting are implemented using a computer.

17. The method of claim 16, wherein the acts of arranging, traversing and sifting are implemented using a computer.

* * * * *

traversing the representation of the graph from the top down to produce a list of the labels in a selected order; and

sifting the variables of the binary decision diagram based on the selected order.

8. (Previously Presented) An apparatus for proving properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine values of the internal signals, the apparatus comprising:

first storage circuitry for storing bits representative of a set of functions which represent the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

a processor that substitutes the functions which determine the values of the internal signals into the set of functions representing the system and detects an increase in a number of the nodes of the binary decision diagram, and in response to the detection, arranges the variables of the binary decision diagram ~~on~~ in a representation of a graph having a top, nodes and leaves, the nodes being labeled with ~~a~~ the set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes, traverses the labels in a selected order and sifts the variables of the binary decision diagram based on the selected order; and

second storage circuitry, wherein the sifted variables of the binary decision diagram are written by the processor to the second storage circuitry.

9. (Previously Amended) The apparatus of claim 8, wherein the number is a threshold derived from an original number of nodes.

10. (Previously Amended) Apparatus as claimed in claim 8, wherein the number is a number of nodes which branch on a predetermined variable.

11. (Previously Amended) The apparatus of claim 8, wherein the number is an absolute number.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,149,663
APPLICATION NO.	:	09/159,748
ISSUE DATE	:	December 12, 2006
INVENTOR(S)	:	Geoff Barrett

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 8, column 8, line 13 should read:
--of the binary decision diagram in a representation of a--

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